128k x 8 nvSRAM

FEATURES

- **High-performance 1Mb non-volatile SRAM**
- **25ns Access Time**
- **10ns Output Enable Access Time**
- **I_{CC} = 10mA typ. at 25 ns Cycle Time**
- **I_{CC} = 2mA typ. at 250 ns Cycle Time**
- **Read Last Successful Written Address**
- **Unlimited Read/Write Endurance**
- **Automatic non-volatile STORE on Power Down or Brown Out (POWERSTORE)**
- **Non-volatile STORE under Soft Sequence or Hardware ($\overline{HSB}$) Control**
- **Automatic RECALL to SRAM on Power Up or after Brown Out**
- **Unlimited RECALL Cycles**
- **100k STORE Cycles**
- **100-Year non-volatile Data Retention**
- **3.0V to 3.6V Power Supply**
- **Commercial and Industrial Temperatures**
- **BGA48 (6x8)**
- **RoHS-Compliant**

DESCRIPTION

The Anvo-Systems Dresden ANV22AA8A is a 1Mb SRAM with a non-volatile SONOS storage element included with each memory cell, organized as 128k words of 8 bits each. There are 2 separate modes of operation: SRAM mode and non-volatile mode. In SRAM mode, the memory operates as an ordinary static RAM. In non-volatile operation mode, data is transferred in parallel from SRAM to the SONOS elements (STORE) or from all of them to SRAM (RECALL). In non-volatile mode SRAM functions are disabled.

The SRAM can be read and written an unlimited number of times, while independent non-volatile data resides in SONOS elements. Data transfers from the SRAM to the SONOS elements take place automatically upon power down or brown out situation (POWERSTORE) using charge stored in a small external capacitor.

Transfers from the SONOS elements to the SRAM (RECALL) take place automatically on power up or may be initiated under user control by a software sequence. Internally, RECALL is a two step procedure. First, the SRAM data is cleared and second, the non-volatile information is transferred into the SRAM cells.

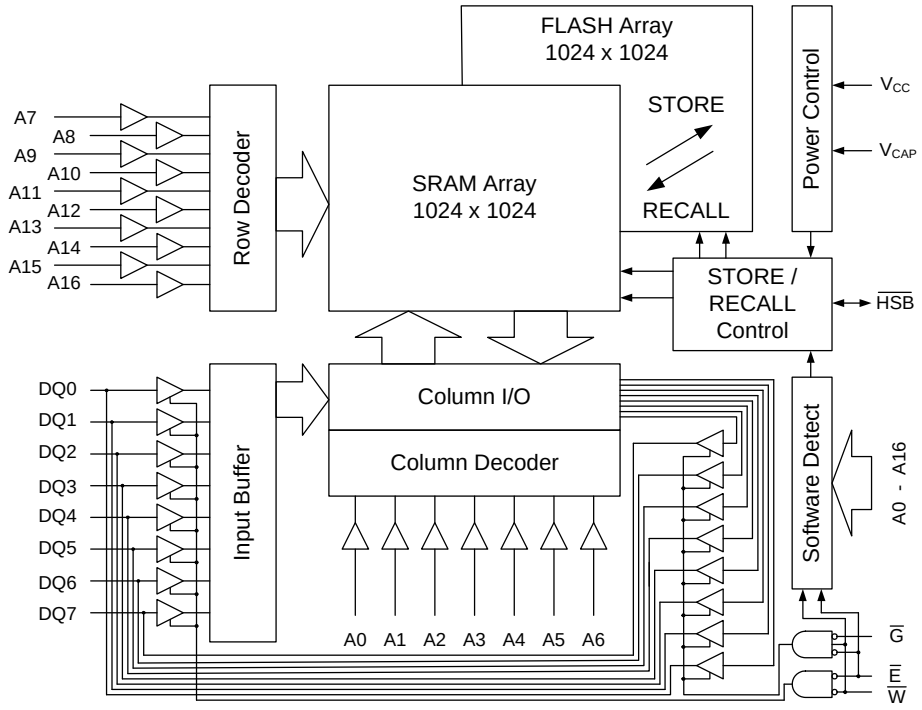
STORE cycles also may be initiated under user control by a software sequence or by a single pin ($\overline{HSB}$).

Once a STORE cycle is initiated, further input or output are disabled until the cycle is completed.

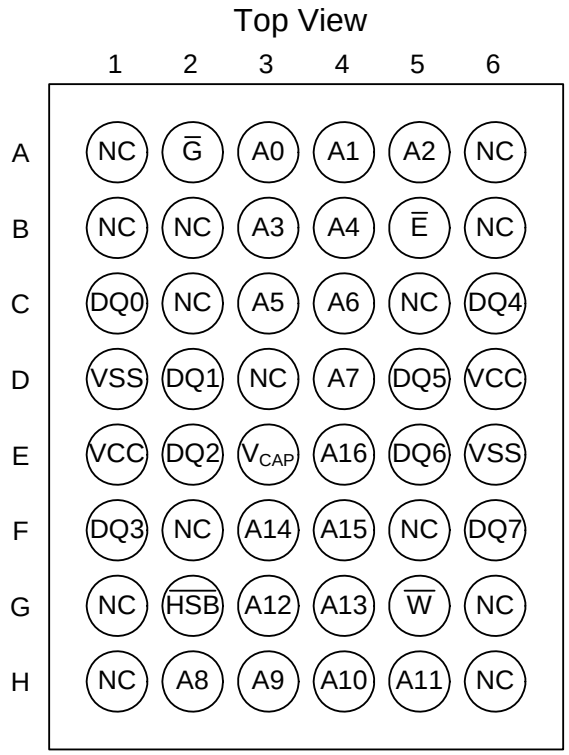
The PowerStore function can also be enabled or disabled by a software sequence.

With Read Last Successful Written Address it is possible to read out the 3 byte of address for data where last WRITE was successful.

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTIONS

Signal Name	Signal Description
A0 - A16	Address Inputs
DQ0 - DQ7	Data In/Out
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Power Supply Voltage
V_{SS}	Ground
V_{CAP}	Capacitor Voltage
$\overline{HSB}$	Hardware Controlled Store/Busy

Device Operation

The ANV22AA8A has two separate modes of operation:
- SRAM mode and
- non-volatile mode.

The memory operates in SRAM mode as a standard fast static RAM. Data is transferred in non-volatile mode from SRAM to SONOS elements (STORE) or from SONOS elements to SRAM (RECALL). In this non-volatile mode SRAM functions are disabled.
STORE cycles may be initiated under user control via a software sequence or $\overline{HSB}$ assertion and are also automatically initiated when the power supply voltage level of the chip falls below V_{SWITCH}. RECALL operations are automatically initiated upon power up and may also occur when the V_{CC} rises above V_{SWITCH}, after a low power condition. RECALL cycles may also be initiated by a software sequence.

Power up

When the power supply is turned on from V_{SS}, Chip Enable ($\overline{E}$) has to follow the V_{CC} voltage in accordance with the definition of V_{IH}. It must not be allowed to float, but could be connected via a suitable pull-up resistor to V_{CC}.
The Chip Enable signal ($\overline{E}$) is edge as well as level sensitive. This ensures that the device becomes deselected after Power-Down until V_{CC} reaches V_{CCmin} and a falling edge of $\overline{E}$ from the V_{IH} level has been detected thereafter. This will start the first operation.

Power On Reset

In order to prevent data corruption and inadvertent WRITE operations during Power-up, all input signals will be ignored and Data Outputs DQ0 - DQ7 will be in high impedance state. Power On Reset is exited when V_{CC} reaches a stable V_{CCmin}. Logical signals can applied.

Power-down / Brown Out

When V_{CC} drops during normal operation below V_{SWITCH} all external operations will be disabled, the device will ignore any input signals and Data Outputs (DQ) will be in high impedance state. Power-down during self timed Store Operation will not corrupt data in the memory. Write operation of the current Byte will be completed independent from the power supply. Prior to any STORE operation the whole data in the non-volatile memory will be erased to allow STORE operation of new and restore of unchanged data.

Operating and Stand-by Modes

When Chip Enable ($\overline{E}$) is Low, the device is enabled. In Operating Mode it is consuming $I_{CC(OP)}$. In the other case, when Chip Enable ($\overline{E}$) is High, the device is in Standby Mode with the reduced Supply Current $I_{CC(SB)}$.

SRAM READ

The ANV22AA8A performs a READ cycle whenever $\overline{E}$ and $\overline{G}$ are LOW and $\overline{HSB}$ and $\overline{W}$ are HIGH. The address specified on pins A0 - A16 determines which of the 128k data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of t_{cR}. If the READ is initiated by $\overline{E}$ or $\overline{G}$, the outputs will be valid at $t_{a(E)}$ or at $t_{a(G)}$,
whichever is later. The data outputs will repeatedly respond to address changes within the t_{cR} access time without the need for transition on any control input pins, and will remain valid until another address change or until $\overline{E}$ or $\overline{G}$ is brought HIGH or $\overline{W}$ or $\overline{HSB}$ is brought LOW.

SRAM WRITE

A WRITE cycle is performed whenever $\overline{E}$ and $\overline{W}$ are LOW and $\overline{HSB}$ is HIGH. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either $\overline{E}$ or $\overline{W}$ goes HIGH at the end of the cycle. The data on pins DQ0 - 7 will be written into the memory if it is valid $t_{su(D)}$ before the end of a $\overline{W}$ controlled WRITE or $t_{su(D)}$ before the end of an $\overline{E}$ controlled WRITE.
It is recommended that $\overline{G}$ is kept HIGH during the entire WRITE cycle to avoid data bus contention on the common I/O lines. If $\overline{G}$ is left LOW, internal circuitry will turn off the output buffers $t_{dis(W)}$ after $\overline{W}$ goes LOW.

POWERSTORE

During normal operation, the ANV22AA8A will draw current from V_{CC} and charge up a capacitor connected to the V_{CAP} pin. If the voltage on the V_{CC} pin drops below V_{SWITCH}, the part will automatically disconnected from V_{CC} and initiate a STORE operation. The charged capacitor on V_{CAP} pin provides the necessary energy for this PowerStore operation.
Figure 1 shows the proper connection of capacitors for automatic STORE operation.

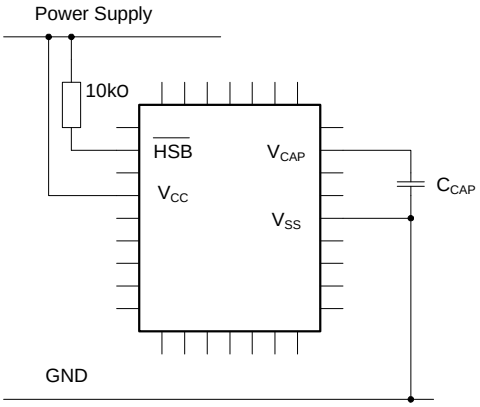


Figure 1: POWERSTORE Operation
Schematic Diagram

Each ANV22AA8A must have its own STORE capacitor. A normal high frequency bypass capacitor between the power supply voltage V_{CC} and V_{SS} is expected.
In order to prevent unneeded STORE operations, automatic STOREs as well as those initiated by externally driving $\overline{HSB}$ LOW will be ignored unless at least one WRITE operation has taken place since the most recent STORE cycle. Note that if $\overline{HSB}$ is driven LOW via external circuitry and no WRITES have taken place, the part will still be disabled until $\overline{HSB}$ is allowed to return HIGH. Software initiated STORE cycles are performed regardless of whether or not a WRITE operation has taken place.
POWERSTORE operation without the external capacitor will damage the volatile and non-volatile content of the memory.

Automatic RECALL

During power up, an automatic RECALL takes place. At a low power condition ($V_{CC} < V_{SWITCH}$) an internal RECALL request may be latched. As soon as power supply voltage exceeds the sense voltage of V_{SWITCH}, a requested RECALL cycle will automatically be initiated and will take $t_{RESTORE}$ to complete.
If the ANV22AA8A is in a WRITE state at the end of power up RECALL, the recalled SRAM data will be overwritten. To help avoid this situation, a 10 kΩ resistor should be connected between $\overline{W}$ or $\overline{E}$ and power supply voltage V_{CC}.

Software non-volatile STORE

The ANV22AA8A software controlled STORE cycle is initiated by executing sequential $\overline{E}$ clocked READ cycles from six specific address locations. By relying on READ cycles only, the ANV22AA8A implements non-volatile operation while remaining compatible with standard 128K x 8 SRAMs. During the STORE cycle, an erase of the previous non-volatile data is performed first, followed by a parallel programming of all non-volatile elements. Once a STORE cycle is initiated, further inputs and outputs are disabled until the cycle is completed.
Because a sequence of addresses is used for STORE initiation, it is important that no other READ or WRITE accesses intervene in the sequence or the sequence will be aborted.
To initiate the STORE cycle the following READ sequence must be performed:

1.	Read address	0x4E38	Valid READ
2.	Read address	0xB1C7	Valid READ
3.	Read address	0x83E0	Valid READ
4.	Read address	0x7C1F	Valid READ
5.	Read address	0x703F	Valid READ
6.	Read address	0x8FC0	Initiate STORE

Once the sixth address in the sequence has been entered, the STORE cycle will commence and the chip will be disabled. It is important that READ cycles and not WRITE cycles are used in the sequence, although it is not necessary that $\overline{G}$ is LOW for the sequence to be valid. After the t_{STORE} cycle time has been fulfilled, the SRAM will again be activated for READ and WRITE operation.

Software non-volatile RECALL

A RECALL cycle is initiated with a sequence of $\overline{E}$ clocked READ operations in a manner similar to the STORE initiation. To initiate the RECALL cycle the following sequence of READ operations must be performed:

1.	Read address	0x4E38	Valid READ
2.	Read address	0xB1C7	Valid READ
3.	Read address	0x83E0	Valid READ
4.	Read address	0x7C1F	Valid READ
5.	Read address	0x703F	Valid READ
6.	Read address	0x4C63	Initiate RECALL

Internally, RECALL is a two step procedure. First, the SRAM data is cleared and second, the non-volatile information is transferred into the SRAM cells. The RECALL operation in no way alters the data in the SONOS cells. The non-volatile data can be recalled an unlimited number of times.

$\overline{HSB}$ non-volatile STORE

The hardware controlled STORE Busy pin ($\overline{HSB}$) is connected to an open drain circuit acting as both input and output to perform two different functions. When driven LOW by the internal chip circuitry it indicates that a STORE operation (initiated via any means) is in progress within the chip. When driven LOW by external circuitry for longer than $t_{w(H)S}$, the chip will conditionally initiate a STORE operation after $t_{dis(H)S}$.
READ and WRITE operations that are in progress when $\overline{HSB}$ is driven LOW (either by internal or external circuitry) will be allowed to complete before the STORE operation is performed, in the following manner.
After $\overline{HSB}$ goes LOW, the part will continue normal SRAM operation for $t_{dis(H)S}$. During $t_{dis(H)S}$, a transition on any address or control signal will terminate SRAM operation and cause the STORE to commence.
Note that if an SRAM WRITE is attempted after $\overline{HSB}$ has been forced LOW, the WRITE will not occur and the STORE operation will begin immediately.
HARDWARE-STORE-BUSY ($\overline{HSB}$) is a high speed, low drive capability bidirectional control line.
In order to allow a bank of ANV22AA8A's to perform synchronized STORE functions, the $\overline{HSB}$ pin from a number of chips may be connected together. Each chip contains a small internal current source to pull $\overline{HSB}$ HIGH when it is not being driven LOW. To decrease the sensitivity of this signal to noise generated on the PC board, it may optionally be pulled to power supply via an external resistor with a value such that the combined load of the resistor and all parallel chip connections does not exceed $I_{\overline{HSB}OL}$ at V_{OL} (see Figure 1).
Only if $\overline{HSB}$ is to be connected to external circuits, an external pull-up resistor should be used.
During any STORE operation, regardless of how it was initiated, the ANV22AA8A will continue to drive the $\overline{HSB}$ pin LOW, releasing it only when the STORE is complete.
Upon completion of a STORE operation, the part will be disabled until $\overline{HSB}$ actually goes HIGH.

Hardware Protection

The ANV22AA8A offers hardware protection against inadvertent STORE operation during low voltage conditions. When $V_{CC} < V_{SWITCH}$, all software or $\overline{HSB}$ initiated STORE operations will be inhibited.

Disabling Power STORES

If the POWERSTORE function is not required, this feature can be disabled by a soft-sequence.
In this case it is important that no other READ or WRITE accesses intervene in the sequence or the sequence will be aborted.
To initiate POWERSTORE disable the following READ sequence must be performed:

1.	Read address	0x4E38	Valid READ
2.	Read address	0xB1C7	Valid READ
3.	Read address	0x83E0	Valid READ
4.	Read address	0x7C1F	Valid READ
5.	Read address	0x703F	Valid READ
6.	Read address	0x8B45	PowerStore disabled

Once the sixth address in the sequence has been entered, the internal register is set volatile to POWERSTORE = disable. With a Software controlled non-volatile STORE this register takes the status non-volatile. It is not necessary that $\overline{G}$ is LOW for the sequence to be valid.

Enabling Power Stores

If the POWERSTORE function is requested again an activation via a Soft Sequence can occur,
To initiate POWERSTORE enable again the following READ sequence must be performed:

1.	Read address	0x4E38	Valid READ
2.	Read address	0xB1C7	Valid READ
3.	Read address	0x83E0	Valid READ
4.	Read address	0x7C1F	Valid READ
5.	Read address	0x703F	Valid READ
6.	Read address	0x4B46	PowerStore enabled

Once the sixth address in the sequence has been entered, the internal reister is set volatile to POWERSTORE = enable. With a Software controlled non-volatile STORE this register takes the status non-volatile. It is not necessary that $\overline{G}$ is LOW for the sequence to be valid.

Read Last Successful Written Address

An internal register monitors continuously all WRITE addresses. With each successful WRITE it will be set to the address of this operation. It is a 3byte register which is volatile during normal operation. If POWERSTORE is enabled it will be stored in case of power down or brown out like any other data in the memory array. After Power Up the content can be read out via a soft sequence. With the first WRITE the register will be overwritten volatile and with the first STORE operation also non-volatile. With any RECALL also the volatile content of the Read Last Successful Written Address register will be cleared and set to the non-volatile content of the register.
To initiate read out Read Last Successful Written Address register the following READ sequence must be performed:

1.	Read address	0x4E38	Valid READ
2.	Read address	0xB1C7	Valid READ
3.	Read address	0x83E0	Valid READ
4.	Read address	0x7C1F	Valid READ
5.	Read address	0x703F	Valid READ
6.	Read address	0x0D30	*READ Byte high*
7.	Read address	0x4E38	Valid READ
8.	Read address	0xB1C7	Valid READ
9.	Read address	0x83E0	Valid READ
10.	Read address	0x7C1F	Valid READ
11.	Read address	0x703F	Valid READ
12.	Read address	0x4D30	*Read Byte 2*
13.	Read address	0x4E38	Valid READ
14.	Read address	0xB1C7	Valid READ
15.	Read address	0x83E0	Valid READ
16.	Read address	0x7C1F	Valid READ
17.	Read address	0x703F	Valid READ
18.	Read address	0x2D30	*Read Byte low*

Byte high is the upper address, followed by byte 2 and byte low for lowest part of the address.

Low Average Active Power

The ANV22AA8A has been designed to draw significantly less power when $\overline{E}$ is LOW (chip enabled) but the access cycle time is longer than 25 ns.
When $\overline{E}$ is HIGH the chip consumes only standby current.
The overall average current drawn by the part depends on the following items:

1. CMOS or TTL input levels
2. the time during which the chip is disabled ($\overline{E}$ HIGH)
3. the cycle time for accesses ($\overline{E}$ LOW)
4. the ratio of READ to WRITE operation
5. the operating temperature
6. the power supply voltage level

ABSOLUTE MAXIMUM RATINGS[a]

Voltage on Input Relative to Ground . . . . . –0.5V to 4.1V
Voltage on Input Relative to V_{CC} . . . . . –0.5V to (V_{CC} + 0.5V)
Temperature under Bias . . . . . –55°C to 125°C
Storage Temperature . . . . . –65°C to 150°C
Power Dissipation 0.5W
DC Output Current (1 output at a time, 1s duration) 15mA
Maximum accumulated storage time at 150°C . . . . . 0.5 years
Maximum accumulated time under Bias at 125°C . . . . . 0.5 years
Static discharge voltage (HBM) . . . . . > 2kV
Latch up current . . . . . > 100mA

a: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Conditions

Symbol	Parameter	ANV22AA8A		Unit
		Min.	Max.	
V_{CC}	Operating Voltage	3.0	3.6	V

DC CHARACTERISTICS (V_{CC} / V = 3.0 - 3.6)

SYMBOL	PARAMETER	COMMERCIAL		INDUSTRIAL		UNITS	NOTES
		MIN	MAX	MIN	MAX		
I_{CC_1}[a]	Average V_{CC} Current at 25ns		20		20	mA	READ to WRITE ratio 1:1 $V_{IN} \le 0.2V_{CC}$ or $\ge 0.8V_{CC}$ I_{OUT} = 0 mA
I_{CC_2}[b]	Average V_{CC} Current during *STORE*		2		2	mA	All Inputs Don’t Care, V_{CC} = max
I_{CC_3}[a]	Average V_{CC} Current at 250 ns		3		3	mA	READ to WRITE ratio 1:1, $V_{IN} \le 0.2V_{CC}$ or $\ge 0.8V_{CC}$
I_{SB_1}[c]	Average V_{CC} Current Standby		2		2	mA	$\overline{E} \ge V_{IH}$, Cycling input levels
I_{SB_2}[c]	V_{CC} Standby Current		0,4		0,4	mA	$\overline{E} \ge (V_{CC} - 0.2V)$ All Others $V_{IN} \le 0.2V$ or $\ge (V_{CC} - 0.2V)$
I_{ILK}	Input Leakage Current		±3		±3	µA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off-State Output Leakage Current		±3		±3	µA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}, $\overline{E}$ or $\overline{G} \ge V_{IH}$
V_{IH}	Input Logic “1” Voltage	$0.8V_{CC}$	V_{CC} + 0.5	$0.8V_{CC}$	V_{CC} + 0.5	V	All Inputs
V_{IL}	Input Logic “0” Voltage	V_{SS} – 0.5	$0.2V_{CC}$	V_{SS} – 0.5	$0.2V_{CC}$	V	All Inputs
V_{OH}	Output Logic “1” Voltage	V_{CC}-0.5		V_{CC}-0.5		V	I_{OUT} = – 2.0 mA
V_{OL}	Output Logic “0” Voltage		0.4		0.4	V	I_{OUT} = 4 mA
T_A	Operating Temperature	0	70	-40	85	°C	
V_{CAP}	Storage Capacitor	48	100	48	100	µF	6.3V
NV_C	non-volatile STORE operations	100		100		K	
$DATA_R$	Data Retention	100		100		Years	@55 °C

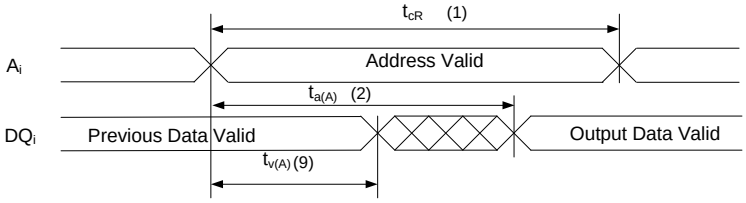
Note a: I_{CC_1} and I_{CC_3} are dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.
Note b: I_{CC_2} is the average current required for the duration of the respective *STORE* cycles (t_{STORE}).
Note c: $\overline{E} \ge V_{IH}$ will not produce standby current levels until any non-volatile cycle in progress has timed out.

SRAM Operation

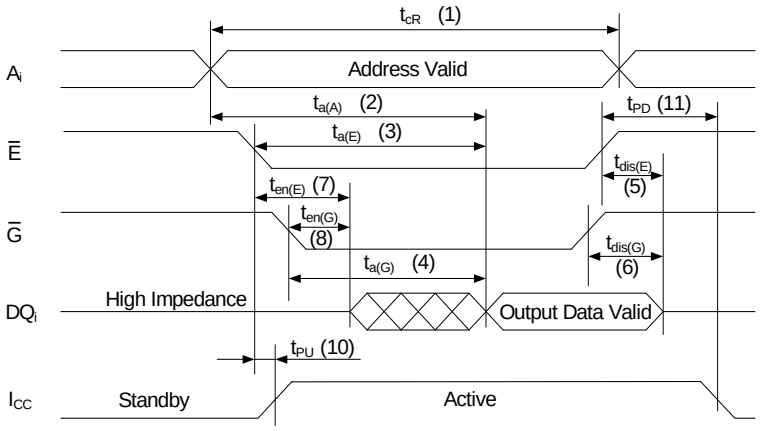
No.	Switching Characteristics	Symbol		Min.	Max.	Unit
		Alt.	IEC			
1	Read Cycle Time[f]	t_{AVAV}	t_{cR}	25		ns
2	Address Access Time to Data Valid[g]	t_{AVQV}	$t_{a(A)}$		25	ns
3	Chip Enable Access Time to Data Valid	t_{ELQV}	$t_{a(E)}$		25	ns
4	Output Enable Access Time to Data Valid	t_{GLQV}	$t_{a(G)}$		10	ns
5	$\overline{E}$ HIGH to Output in High-Z[h]	t_{EHQZ}	$t_{dis(E)}$		10	ns
6	$\overline{G}$ HIGH to Output in High-Z[h]	t_{GHQZ}	$t_{dis(G)}$		10	ns
7	$\overline{E}$ LOW to Output in Low-Z	t_{ELQX}	$t_{en(E)}$	5		ns
8	$\overline{G}$ LOW to Output in Low-Z	t_{GLQX}	$t_{en(G)}$	0		ns
9	Output Hold Time after Address Change	t_{AXQX}	$t_{v(A)}$	3		ns
10	Chip Enable to Power Active[e]	t_{ELICCH}	t_{PU}	0		ns
11	Chip Disable to Power Standby[d, e]	t_{EHICCL}	t_{PD}		25	ns
12	Write Cycle Time	t_{AVAV}	t_{cW}	25		ns
13	Write Pulse Width	t_{WLWH}	$t_{w(W)}$	20		ns
14	Write Pulse Width Setup Time	t_{WLEH}	$t_{su(W)}$	20		ns
15	Address Setup Time	t_{AVWL}	$t_{su(A)}$	0		ns
16	Address Valid to End of Write	t_{AVWH}	$t_{su(A-WH)}$	20		ns
17	Chip Enable Setup Time	t_{ELWH}	$t_{su(E)}$	20		ns
18	Chip Enable to End of Write	t_{ELEH}	$t_{w(E)}$	20		ns
19	Data Setup Time to End of Write	t_{DVWH}	$t_{su(D)}$	10		ns
20	Data Hold Time after End of Write	t_{WHDX}	$t_{h(D)}$	0		ns
21	Address Hold after End of Write	t_{WHAX}	$t_{h(A)}$	0		ns
22	$\overline{W}$ LOW to Output in High-Z[h, i]	t_{WLQZ}	$t_{dis(W)}$		10	ns
23	$\overline{W}$ HIGH to Output in Low-Z	t_{WHQX}	$t_{en(W)}$	5		ns

e: . Parameter guaranteed but not tested.
f: . Device is continuously selected with $\overline{E}$ and $\overline{G}$ both LOW.
g: . Address valid prior to or coincident with $\overline{E}$ transition LOW.
h: . . Measured ± 200 mV from steady state output voltage.
i:. . . If $\overline{W}$ is LOW and when $\overline{E}$ goes LOW, the outputs remain in the high impedance state.
j:. . . $\overline{E}$ or $\overline{W}$ must be V_{IH} during address transition.

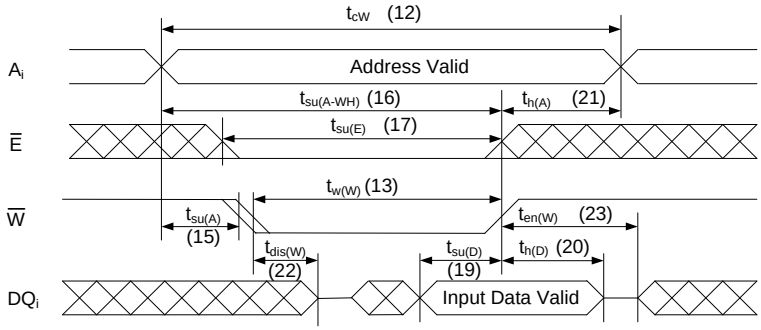
Read Cycle 1: Ai-controlled (during Read cycle: $\overline{E} = \overline{G} = V_{IL}$, $\overline{W} = V_{IH}$)[f]



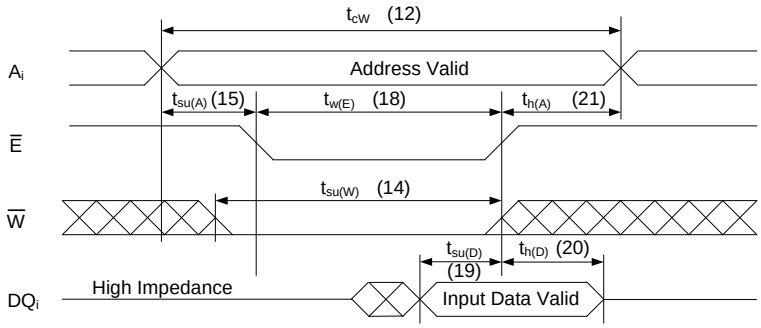
Read Cycle 2: $\overline{G}$-, $\overline{E}$-controlled (during Read cycle: $\overline{W} = V_{IH}$)[g]



Write Cycle #1: $\overline{W}$-controlled[j]



Write Cycle #: $\overline{E}$-controlled[j]



Nonvolatile Memory Operations

Mode Selection

E	W	HSB	A16 - A0	Mode	I/O	Power	Notes
H	X	H	X	Not Selected	Output High Z	Standby	
L	H	H	X	Read SRAM	Output Data	Active	l
L	L	H	X	Write SRAM	Input Data	Active	
L	H	H	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x8FC0	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile STORE	Output Data Output Data Output Data Output Data Output Data Output High Z	Active	k, l k, l k, l k, l k, l k
L	H	H	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x4C63	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile RECALL	Output Data Output Data Output Data Output Data Output Data Output High Z	Active	k, l k, l k, l k, l k, l k
L	H	H	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x8B45	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Automatic STORE disabled	Output Data Output Data Output Data Output Data Output Data Output High Z	Active	k, l k, l k, l k, l k, l k
L	H	H	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x4B46	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Automatic STORE enabled	Output Data Output Data Output Data Output Data Output Data Output High Z	Active	k, l k, l k, l k, l k, l k
X	X	L	X	STORE/Inhibit	Output High Z	ICC2/Standby	m

k: The six consecutive addresses must be in order listed above for a Store, for a RECALL cycle or for Power STORE disable / enable. $\overline{W}$ must be high during all six consecutive cycles. For mode selection only the addresses A2 -A14 will be used. Addresses A0, A1, A15 and A16 are don't care. See STORE cycle, RECALL cycle, Power STORE disable / enable tables and diagrams for further details.

l: I/O state assumes that $\overline{G}$ =V_{IL}. Activation of non-volatile cycles does not depend on the state of $\overline{G}$.

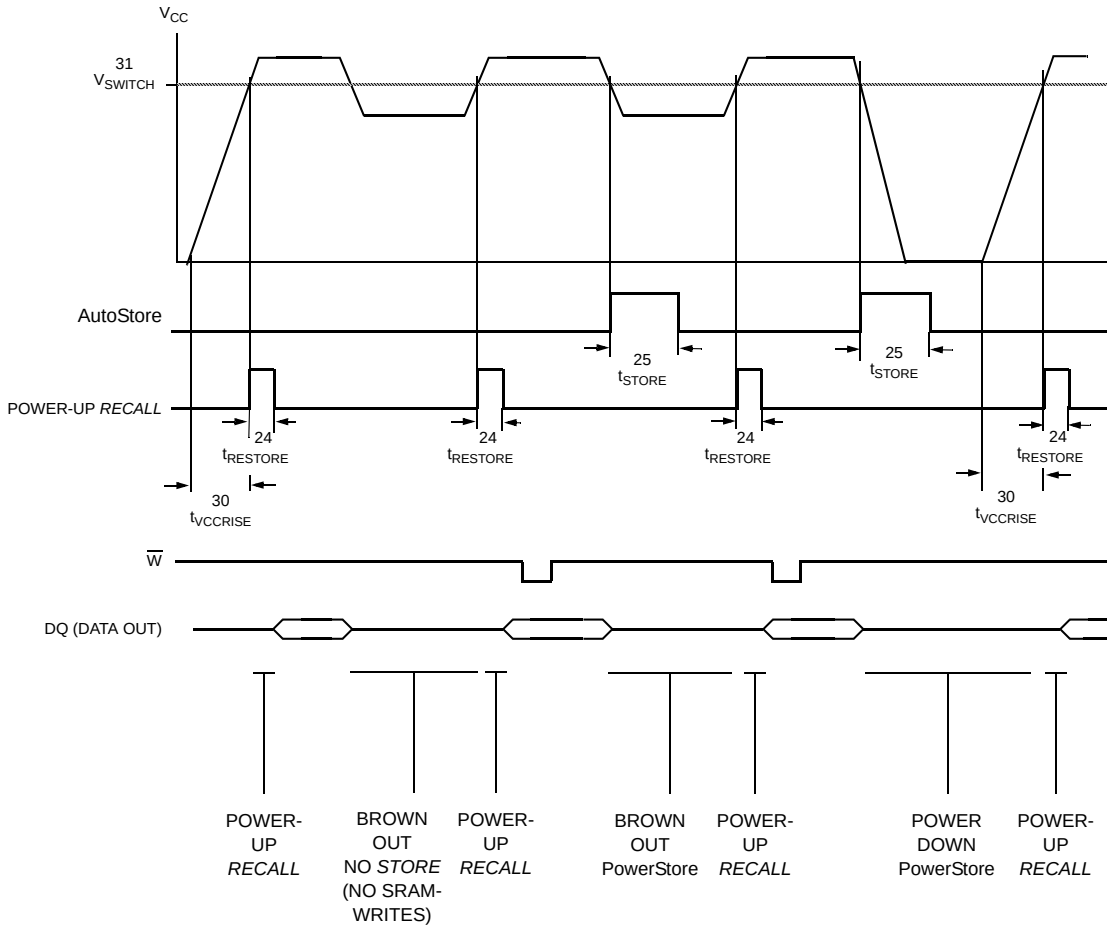
m: $\overline{HSB}$ initiated STORE operation actually occurs only if a WRITE has been done since last STORE operation and Automatic STORE is anabled. After the STORE (if any) completes, the part will go into standby mode inhibiting all operation until $\overline{HSB}$ rises.

No.	Power Up RECALL / Hardware Controlled STORE	Symbol		Min.	Max.	Unit
		Alt.	IEC			
24	Power Up RECALL Duration[n, e]	$t_{RESTORE}$			200	µs
25	STORE Cycle Duration Automatic STORE	t_{STORE}			8	ms
26	STORE Cycle Duration HSB controlled	t_{HLQX}	$t_{d(H)S}$		8	ms
27	$\overline{HSB}$ Low to Inhibit On[e]	t_{HLQZ}	$t_{dis(H)S}$	50		ns
28	$\overline{HSB}$ High to Inhibit Off[e]	t_{HHQX}	$t_{en(H)S}$		50	ns
29	External STORE Pulse Width[e]	t_{HLHX}	$t_{w(H)S}$	20		ns
30	$\overline{HSB}$ Output Low Current[e,o]	$I_{\overline{HSB}OL}$		3		mA
31	V_{CC} Power Up Rise Time	$t_{VCCRISE}$		100		µs
32	$\overline{HSB}$ Output High Current[e, o]	$I_{\overline{HSB}OH}$		5	60	µA
33	Low Voltage Trigger Level	V_{SWITCH}		2.35	2.65	V

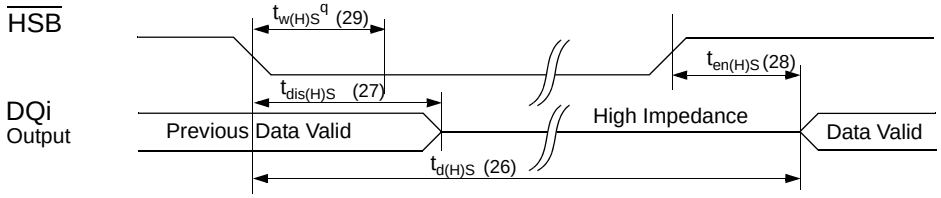
n: $t_{RESTORE}$ starts from the time V_{CC} rises above V_{SWITCH}.

o: $\overline{HSB}$ is an I/O that has a week internal pullup; it is basically an open drain output. It is meant to allow up to 8 ANV22AA8A to be ganged together for simultaneous storing. Do not use $\overline{HSB}$ to pullup any external circuitry other than other ANV22AA8A $\overline{HSB}$ pins.

Automatic STORE and Power UP RECALL



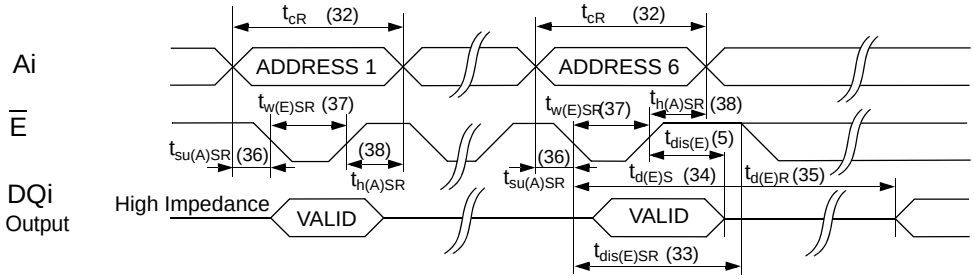
Hardware Controlled STORE



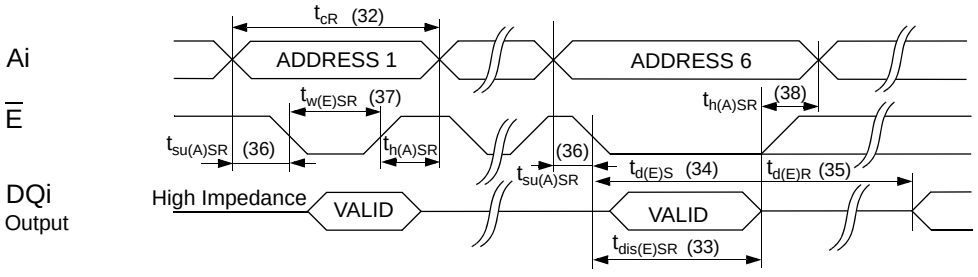
No.	Software Controlled STORE / RECALL and AutomaticSTORE enable / disable Cycle	Symbol		Min.	Max.	Unit
		Alt.	IEC			
32	STORE / RECALL Initiation Time	t_{AVAV}	t_{cR}	25		ns
33	Chip Enable to Output Inactive[s]	t_{ELQZ}	$t_{dis(E)SR}$		25	ns
34	STORE Cycle Time	t_{ELQXS}	$t_{d(E)S}$		8	ms
35	RECALL Cycle Time[r]	t_{ELQXR}	$t_{d(E)R}$		50	µs
36	Address Setup to Chip Enable[t]	t_{AVELN}	$t_{su(A)SR}$	0		ns
37	Chip Enable Pulse Width[s, t]	t_{ELEHN}	$t_{w(E)SR}$	20		ns
38	Chip Disable to Address Change[t]	t_{EHAXN}	$t_{h(A)SR}$	0		ns

p: $t_{PDSTORE}$ approximate $t_{d(E)S}$ or $t_{d(H)S}$; t_{DELAY} approximate $t_{dis(H)S}$.
q: After $t_{w(H)S}$ HSB is hold down internal by STORE operation.
r: An automatic RECALL also takes place at power up, starting when V_{CC} exceeds V_{SWITCH} and takes $t_{RESTORE}$. V_{CC} must not drop below V_{SWITCH} once it has been exceeded for the RECALL to function properly.
s: Once the software controlled STORE or RECALL cycle is initiated, it completes automatically, ignoring all inputs.
t: Noise on the $\overline{E}$ pin may trigger multiple READ cycles from the same address and abort the address sequence.

Software Controlled STORE/RECALL Cycle[t, u, v, w] ($\overline{E}$ = HIGH after STORE initiation)

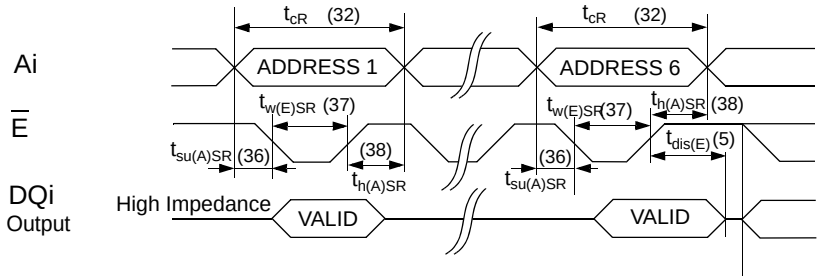


Software Controlled STORE/RECALL Cycle[t, u, v, w] ($\overline{E}$ = LOW after STORE initiation)

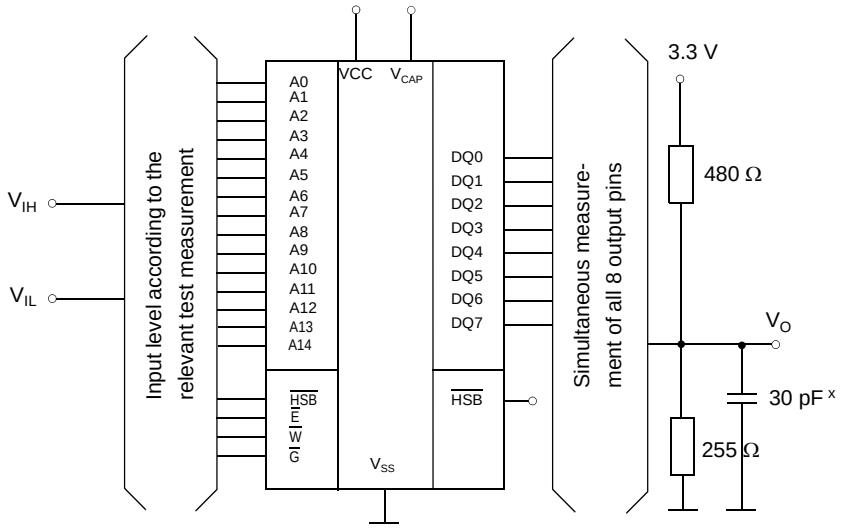


u: If the chip enable pulse width is less then $t_{a(E)}$ (see READ cycle) but greater than or equal to $t_{w(E)SR}$, then the data may not be valid at the end of the low pulse, however the STORE or RECALL will still be initiated.
v: $\overline{W}$ must be HIGH when $\overline{E}$ is LOW during the address sequence in order to initiate a nonvolatile cycle. $\overline{G}$ may be either HIGH or LOW throughout. Addresses 1 through 6 are found in the mode selection table. Address 6 determines whether the ANV22AA8A performs a STORE or RECALL.
w: $\overline{E}$ must be used to clock in the address sequence for the software controlled STORE and RECALL cycles.

Software Controlled PowerSTORE enable / disable Cycle[t, u, v, w]



AC TEST CONDITIONS



x: In measurement of t_{dis}-times and t_{en}-times the capacitance is 5 pF.
y: Between V_{CC} and V_{SS} must be connected a high frequency bypass capacitor 0.1 µF to avoid disturbances.

CAPACITANCE[d]

Capacitance[e]	Conditions	Symbol	Min.	Max.	Unit
Input Capacitance	V_{CC} = 3.3 V V_I = V_{SS} f = 1 MHz T_a = 25 °C	C_I		8	pF
Output Capacitance		C_O		7	pF

Note d: These parameters are guaranteed but not tested.

Product Versions

The ANV22AA8A will be available with the feature sets:

- Supply voltage range 3.0 to 3.6V
- Automatic STORE enabled

Initial Delivery State

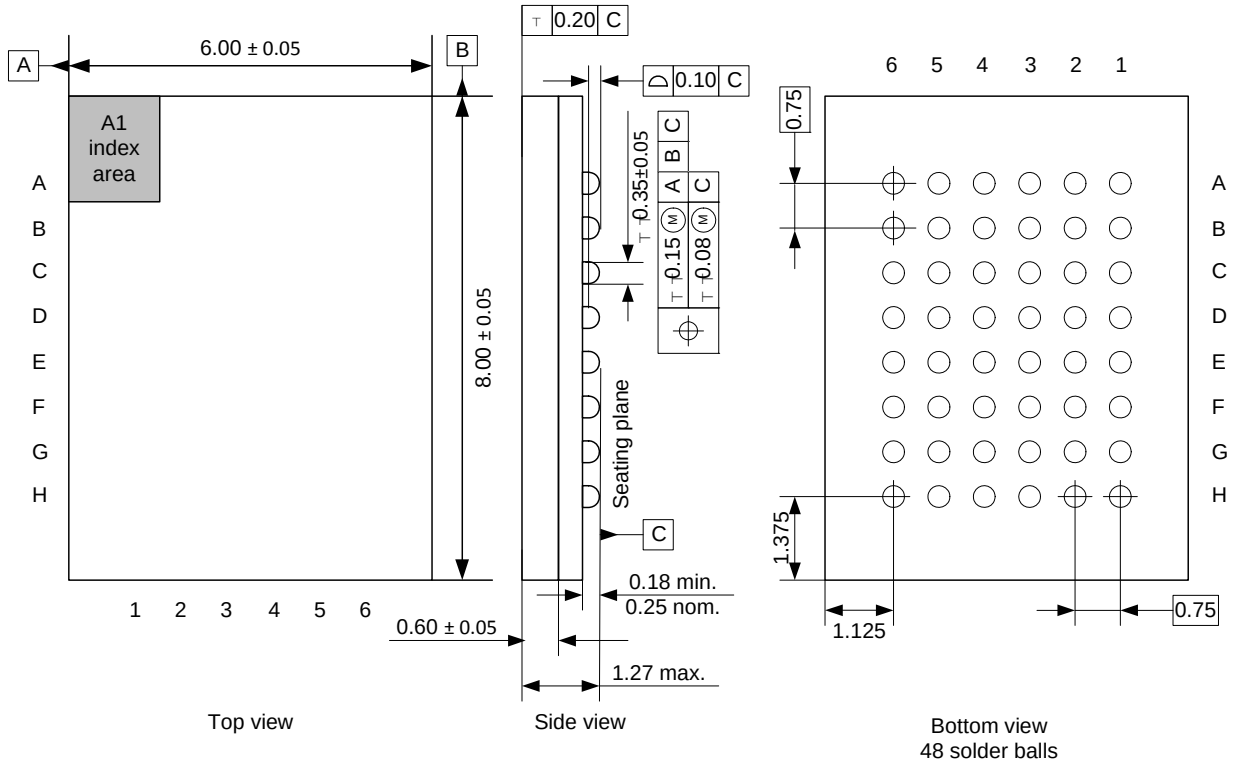
The device is delivered with non-volatile memory array „0“.

NOISE CONSIDERATIONS

The ANV22AA8A is a high-speed memory and so must have a high-frequency bypass capacitor of approximately 0.1µF connected between V_{CC} and V_{SS}, using leads and traces that are as short as possible. As with all high-speed CMOS ICs, normal careful routing of power, ground and signals will help prevent noise problems.

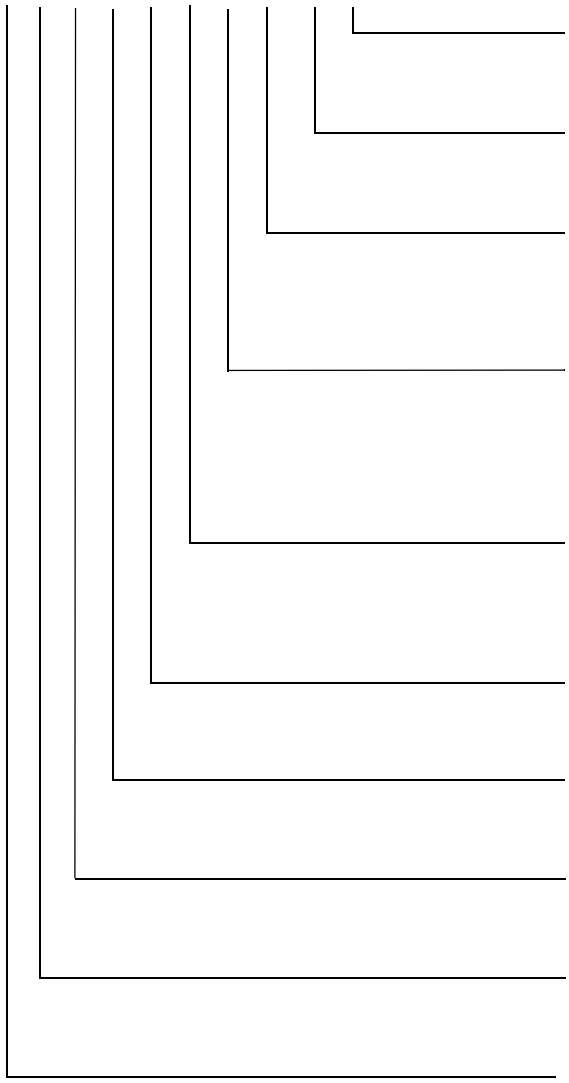
Package

BGA48 (6x8)



Ordering Information

ANV 2 2 A A 8 A B C 25 _



Lead Finish
Blank = SAC105

Access Time
25 = 25ns

Temperature Range
C = Commercial (0 to 70°C)
K = Industrial (-40 to 85°C)

Package
B = BGA

Power Supply
A = 3.0V ... 3.6V

Data Bus
8 = 8bit

Density
A= 1Mb

Version
A = initial

Store Type
2 = PowerStore

Memory Type
2= parallel nvSRAM

Document Revision History

Revision	Date	Summary
1.0	**September 2018**	initial version

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Anvo-Systems Dresden:

ANV22AA8ABC25 R ANV22AA8ABK25 R ANV22AA8ABC25 T ANV22AA8ABK25 T